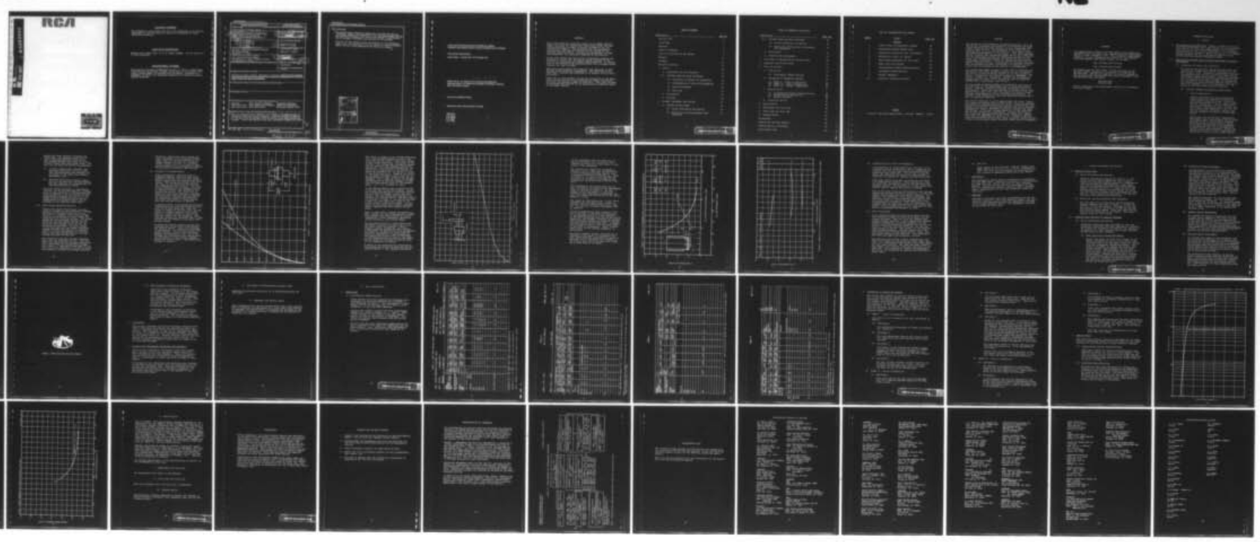
AD-A053 089 RCA CORP LANCASTER PA SSD-ELECTRO-OPTICS AND DEVICES F/6 9/1
MANUFACTURING METHODS ANC TECHNOLOGY (MM AND T) MEASURE FOR FAB--ETC(U)
JAN 78 B B ADAMS, S W KESSLER, R E REED DAAB07-76-C-8120

UNCLASSIFIED NL

| OF |

AD
A053089



END
DATE
FILMED
6 -78
DDC

RCA

DISCLAIMER STATEMENT

The findings in this report are not to be construed as an official Department of the Army position unless so designated by other authorized documents.

DISPOSITION INSTRUCTIONS

Destroy this report when it is no longer needed. Do not return it to the originator.

ACKNOWLEDGEMENT STATEMENT

This project has been accomplished as part of the U.S. Army (Manufacturing and Technology) Program, which has as its objective the timely establishment of manufacturing processes, techniques or equipment to insure the efficient production of current or future defense programs.

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: Fifth Quarterly Progress Report ✓ — 2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle): 6 Manufacturing Methods and Technology (MM&T) Measure for Fabrication and of Silicon Transcalent Thyristor.	5. TYPE OF REPORT & PERIOD COVERED: progress 9 Quarterly Report. no. 5, 1 Oct [redacted]-31 Dec [redacted]77
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s): 10 B. B./Adams, S. W./Kessler, R. E./Reed D. R./Trout	8. CONTRACT OR GRANT NUMBER(s): 15 DAAB07-76-C-8120
9. PERFORMING ORGANIZATION NAME AND ADDRESS: RCA Corp., SSD-Electro Optics & Devices ✓ New Holland Avenue Lancaster, PA 17604	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: Project No. 2769732
11. CONTROLLING OFFICE NAME AND ADDRESS: U.S. Army Electronics Command Production Div., Prod. Integration Branch Ft. Monmouth, NJ 07703	12. REPORT DATE: 11 Jan[redacted]78
	13. NUMBER OF PAGES: 60 12 48 p.
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15. SECURITY CLASS. (of this report): Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited, ~~except that the information presented is not to be construed as a license to manufacture or sell the device described without permission.~~

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Thyristor	Power Switching Component	Transcalent Thyristor
High Current SCR	Power Conditioning Component	Production Engineering
Heat-Pipe Cooling	Solid State Device	Electrical Testing of SCR

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This fifth Quarterly Report describes the progress on the MM&TE program for Transcalent (Heat-Pipe cooled) thyristors. Production engineering measures for the device and the pertinent state-of-the-art on the sample devices are included. Initial test results on the first confirmatory samples are listed.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

4-1∅ 148

20. (Continued)

The present status includes the submission of the Test Plan for the confirmatory samples, the fabrication of the confirmatory sample devices, the engineering analyses of the initial test results on these devices, and the equipment refinements being procured for this program.

Plans for the next Quarter include the conclusion of the confirmatory sample phase, the preparation of the Test Report for these confirmatory samples, as well as the preparations for the pilot run phase.

ACCESSION for

NTIS	White Section	☑
DDC	Buff Section	☐
UNANNOUNCED		☐
JUSTIFICATION		

BY

DISTRIBUTION/AVAILABILITY CODES

Dist.	AVAIL. and/or	SPECIAL
A		

MANUFACTURING METHODS AND TECHNOLOGY (MM&T) MEASURE FOR FABRICATION OF SILICON TRANSCALENT THYRISTOR

Fifth Quarterly Progress Report

Period Covered: 1 October 1977 to 31 December 1977

Object of Study: The objective of this manufacturing methods and technology measure is to establish the technology and capability to fabricate Silicon Transcalent Thyristors.

Contract No. DAAB07-76-C-8120

Approved for public release; distribution unlimited

Prepared by:
B. B. Adams
S. W. Kessler
R. E. Reed
D. R. Trout

ABSTRACT

This fifth quarterly technical report on the MM&TE Contract DAAK07-76-C-8120 for Transcalent (Heat-Pipe cooled) SCR Thyristors describes progress on device refinements for the Confirmatory Samples. Also described are the problems encountered and the results achieved in the testing of the numerous characteristics, including the measurement of some new parameters, not previously required by the contract.

Actual test results for the initial confirmatory samples are included to verify that the device design conforms to the electrical, mechanical and thermal specifications. An evaluation to the revised dv/dt characteristics and a package stress analysis are also included.

Additional preparations for production are described as well as some vendor selection information. The revision to the PERT Chart, prepared and submitted on 29 August, 1977, is still applicable.

Plans for the next quarter include the conclusion of the fabrication and evaluation of the Confirmatory Sample thyristors, utilizing the recently submitted Test Plan. This plan includes the proposed modification to the specification submitted early in the report period.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS AND TABLES

PURPOSE

The purpose of this production engineering contract is to establish the technology and capability to fabricate heat-pipe cooled semiconductor power devices, silicon Transcalent Thyristors, Type J-15371. The subsequent pilot production of these devices is a part of the contract. This report covers the efforts performed by the contractor in the fifth quarterly period to modify the engineering sample device for production, use the established process and fabrication methods to construct the confirmatory samples and adequately characterize these sample thyristors. Plans for future work are also presented, corrective action is delineated for problems that have been encountered and other information is discussed to help assure that the purpose of the contract is accomplished.

This contractual MM&TE program is being used to establish the production techniques, establish quality control procedures and verify a pilot production capability for the J-15371 thyristor, conforming to the drawing attached to AMENDMENT 1 of SCS-477. Electrical, mechanical, thermal and environmental inspections are a part of the program as well as extensive documentation requirements, per DD 1423.

No high volume production facilities existed at the start of this contract for the Transcalent type of solid-state power device. However, production planning constitutes Step II of the contract. Thus, the time required to produce future large quantities of the J-15371 will be reduced for either current military requirements or future emergency requirements. Reduction of the reproductive costs for production quantities is also an important objective.

The J-15371 thyristor is a 400 amperes RMS, 800 volts, forced air cooled solid-state power control device, utilizing integral heat-pipes for improved cooling efficiency, lighter weight and smaller size than the conventional devices with their externally attached heat-sinks. Improved reliability results from these innovations. A blocking voltage capability of 800 volts minimum at 125° Celsius is a requirement. Original R&D efforts were conducted successfully by RCA under Contract No. DAAK02-69-C-0609, for MERADCOM, Ft. Belvoir, VA. Potential applications include power conditioning, power switching, phase control, voltage variable power supply and motor speed control equipments.

GLOSSARY

All abbreviations, symbols and terms used in this report are consistent with the Electronics Command Technical Requirements SCS-477, dated 5 December, 1974. This Technical Requirements document, in turn, references MIL-S-19500 for the abbreviations and sumbols used therein except, as follows:

V_{GR} = Reverse Gate Voltage

I_{GR} = Reverse Gate Current

The format used for this report is that specified in the DD 1423, namely, ECIPPR No. 15, Appendix C, augmented by MIL-STD-847A. Sub-section numbering is based on Appendix C and the applicable test methods are those referenced in the following military standards:

MIL-STD-750B
MIL-Std-202E

Detail, individual item requirements shall be in accordance with MIL-S-19500.

NARRATIVE AND DATA

1. Device

a. Description of the Structure - Refer to pages 9-13 of the First Quarterly Report for a description of the Transcalent Thyristor device, the applicable reports, and the applicable patents as well as the advantages of this heat-pipe cooled technical approach. Refer to Figure 1 in the Second Quarterly Report for the cross-section drawing of the J-15371 with the external dimensions added.

b,c. Defining the Problem Areas and Work Performed to Resolve the Problem

(1) Conversion of Design for Production

The Transcalent Thyristor design achieved under R&D Contract No. DAAK02-69-C-0609 was described in the FTR, October, 1972. Subsequent refinements have been incorporated under Contract N62269-73-C-0635 and by RCA-funded engineering projects. Additional engineering is being applied under the MM&TE program to convert the design to one more suitable for production, as described in prior Quarterly Reports covering the period 27 September 1976 to 30 September 1977 and below for the most recent quarterly period.

(a) Item No. 0001AB Confirmatory Sample Phase

i. Device Fabrication

Initial candidates for the confirmatory sample phase were constructed during the last quarterly report period. Serial Nos. N12 and N13 passed all of the tests of the Group A Inspections, Group B, Sub-Group 1 and Group C, Sub-Groups 3 and 5 tests. However, after being subjected to the 25°C below zero Group B, Sub-Group 2 tests, both devices degraded in blocking voltage capability.

Serial Nos. N16 and N17 were subsequently fabricated from a new diffusion lot in which the emitters were intentionally diffused shallower than in earlier lots of wafers. This change improved the dv/dt capability of the devices, but with a corresponding increase in the gate currents. During the report period, both devices passed most of the tests of Group A, with a gate current

in Sub-Group 4 that met or exceeded the proposed new maximum limit.

Both N16 and N17 also passed the Group C, Sub-Group 5 thermal resistance test. Unfortunately, after the latter test, No. N17 was found to be degraded in voltage. It was analyzed to determine its failure cause. When the weld ring was cut, the two heat-pipes immediately came apart, indicating the wafer had cracked from edge to edge while testing. The crack traveled 50 percent through the silicon and 50 percent along the surface of the wafer, exposing the nickel plating. The nickel plating was not reflective and did not appear to be wetted by the solder. This partial solder joint to the heat-pipe is believed to have induced asymmetrical stresses in the silicon which, in turn, lead to the devices' failure.

Serial No. N16 continued with the remaining Group A as well as the Group B Inspections in the latest report period. Following 140 hours of operation in the Group B, Sub-Group 4 Blocking Voltage Life Test, N16 unexpectedly degraded in reverse blocking voltage to less than one-half of its original value. The test was discontinued.

This degradation was completely unexpected because six of the engineering samples had been subjected to this test without failure or degradation, as reported in the previous quarterly report. To re-confirm the integrity of the basic design, serial No. N10 was returned to the blocking voltage life test for almost 600 more hours for an overall total of 776 hours without degradation. It was thus concluded that N16 was a random, early life failure that should not recur on future devices.

Device, Ser. No. 18, was fabricated and delivered to test during the report period. Test results for all of these devices are listed in Table 1a, b, c and d of this report.

ii. Silicon Wafer Processing

More devices would have been fabricated in this report period but the wafers processed during the first half of the period had very high gate currents. Some of the wafers exhibited gate currents greater than 1 ampere. Since the diffusion schedule has been changed to produce wafers having higher gate currents, and in turn, a greater dv/dt capability, the first conclusion was that the change in the emitter diffusion schedule was too great. When a second group of wafers also exhibited high gate currents, an analysis was made of the cause.

The cause was found to be unintentional short circuits through the oxide layer covering the gate to emitter junction. These shorts could only be located by applying a coating of beeswax onto the wafers and then passing several amperes of current between the emitter and gate metallized contacts. At the point of a short circuit, sufficient heat was generated to melt the wax. Faults in the oxide insulation due to inadequate photoresist masking could then be identified on the metallographic microscope in the region where the wax had melted. This group of wafers, lot No. 17, had gate currents in excess of the specification and thus, were not suitable for mounting between heat-pipes as confirmatory sample devices.

Corrective action involved the use of redundant photoresist processing for the etching of the oxide/polycrystalline silicon/oxide layers on the wafers. This processing has been instituted on all future lots of wafers. This change has succeeded in eliminating the short circuits.

In redundant processing, one film of photoresist is used to etch the top layer of oxide and the resist is then stripped off. A second film of resist is then used as a chemically-resistant mask when etching the polycrystalline silicon layer. The resist is then removed and the polycrystalline silicon is used as a mask to etch the lower oxide layer.

During the first minutes of etching the lower oxide, the residual oxide film on top of the polycrystalline silicon is also removed because that layer of oxide is much thinner than the bottom layer. The top layer of oxide had served two purposes:

(i) It had a strong color contrast with the polycrystalline silicon so that when the photoresist was removed, any pin holes in the oxide were readily observable, and

(ii) The oxide layer had a greater resistance to the etch than the photoresist had when removing the unwanted part of the polycrystalline silicon.

The first wafers processed in this manner (lots No. 19 and 20) have excellent correlations of gate currents to shunting currents. This correlation is an indication that the measured gate currents are now all in the single crystal diffused material and not augmented by any spurious short-circuit currents in the external oxide layer.

iii. High Voltage Blocking Currents

During this report period there was also noted an increase in the blocking or leakage currents of the wafers from lot to lot. This shift in leakage current had not been noted in the diffusion of other wafers for transistor and rectifier devices. The latter wafers are all processed through the same diffusion furnaces except for the one in which the high voltage junctions for the thyristor are diffused. For this reason, it was concluded that the higher thyristor leakage currents may indicate an accumulation of a slight contamination in the diffusion tube used exclusively for the high voltage junctions of the SCRs.

This diffusion tube has now been recleaned and a test lot of wafers was run. The test wafers had improved high voltage characteristics, confirming the contamination assumption, above. It was thus feared that all of the in-pro lots (between No. 19 and 22) would have marginal voltages and leakage currents.

Therefore, additional lots of wafers are being processed in the recleaned furnace tube. They will be identified with lot numbers greater than No. 23. Two additional "clean" lots (No. 24 and 25) are being processed on an accelerated schedule for the next confirmatory MM&T devices.

iv. Analysis of Cracked Wafers

Since successfully completing the engineering samples, there has been a new problem of devices having silicon wafers which cracked while the devices were being tested. The cracks were found to be in the plane of the wafer when the devices were disassembled for analysis. At first, it was believed that the cracking was due to induced stresses from assembling and welding the device. The first unit to crack had been welded employing a greater welding current than was used in welding the engineering samples and, therefore, the device was forced to absorb greater heat and residual stress in welding.

A thorough check of the processes and parts revealed that the weld flanges were not as flat as had been specified. When the flange is welded to the weld ring, the two parts are clamped together, thus introducing a residual stress to flatten and weld the flange into the assembly. This flatness problem was corrected later in the period with the receipt of new parts from another vendor.

To determine whether external forces were cracking the silicon wafer, both tensile and bending moment tests were performed on the package. The tensile test was conducted without a silicon wafer soldered between the heat-pipes, thus, all of the stresses and deflections are indicative of the deformation of the external package around the silicon wafer. The results are plotted in Figure 1.

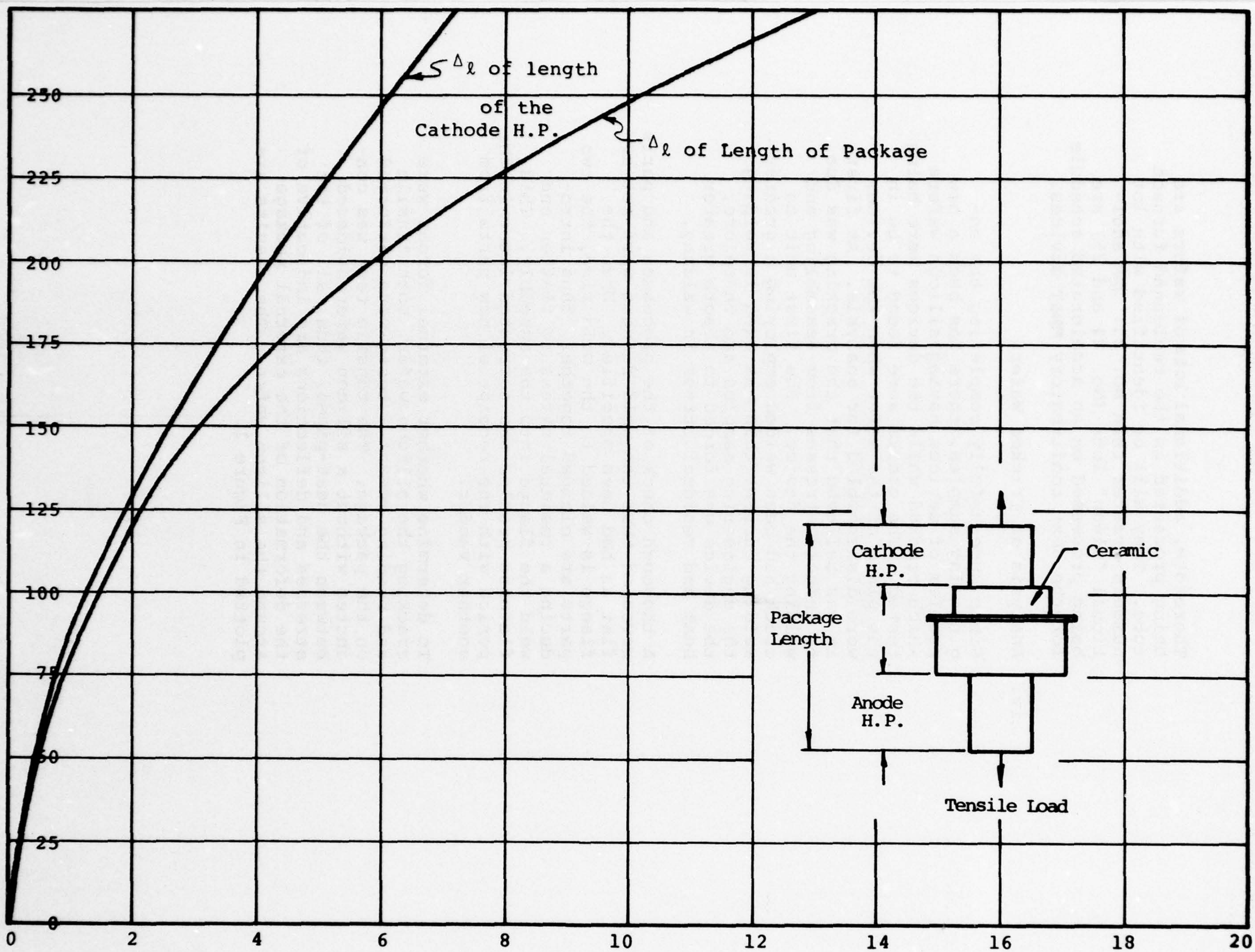


Figure 1 Tensile Test of a Transcalent Package

The change in length of the cathode heat-pipe, H.P., was recorded between the end of the heat-pipe and the flange joining the ceramic to the cathode heat-pipe. The change in the length of the package was recorded by measuring the length of the assembly between the heat-pipes. The difference between the two curves is the deflection of the ceramic to metal seal assembly and the change in length of the anode heat-pipe. Assuming the strain in the anode heat-pipe is small, most all of the deflection is thus occurring in the seal assembly. Up to loads of 125 to 150 pounds, the deflection of the seal assembly is less than the experimental error in the measurements, i.e., 1 to 2 tenths of a mil.

In the bending moment test an operating thyristor was used as the test vehicle. Blocking voltage was applied to the device during the test and the leakage current was monitored to note any change which would be indicative of a cracked wafer. The test results are plotted in Figure 2. The device was bent a total of 0.200 inch with a load of 170 pounds without cracking the wafer. In this test, the heat-pipes were slightly deformed without damaging the more fragile silicon wafer.

Both of these tests, tensile and bending moment, showed that heat-pipes/ceramic to metal seal assembly was strong enough to prevent transmittal of even abnormally applied external stresses to the silicon wafer.

The continuing effort to better define the mechanical stresses which may break a silicon wafer within the package, a finite element computer program was then written to determine the deflection of the molybdenum disc when the assembly is cooled from the soldering temperature to room temperature. The program was written with the thickness of the molybdenum disc as well as the length and the width of the strain isolation ring as the independent variables.

A sketch of the cross-section around which the program was written is shown at the left side of Figure 3. The computed deflection

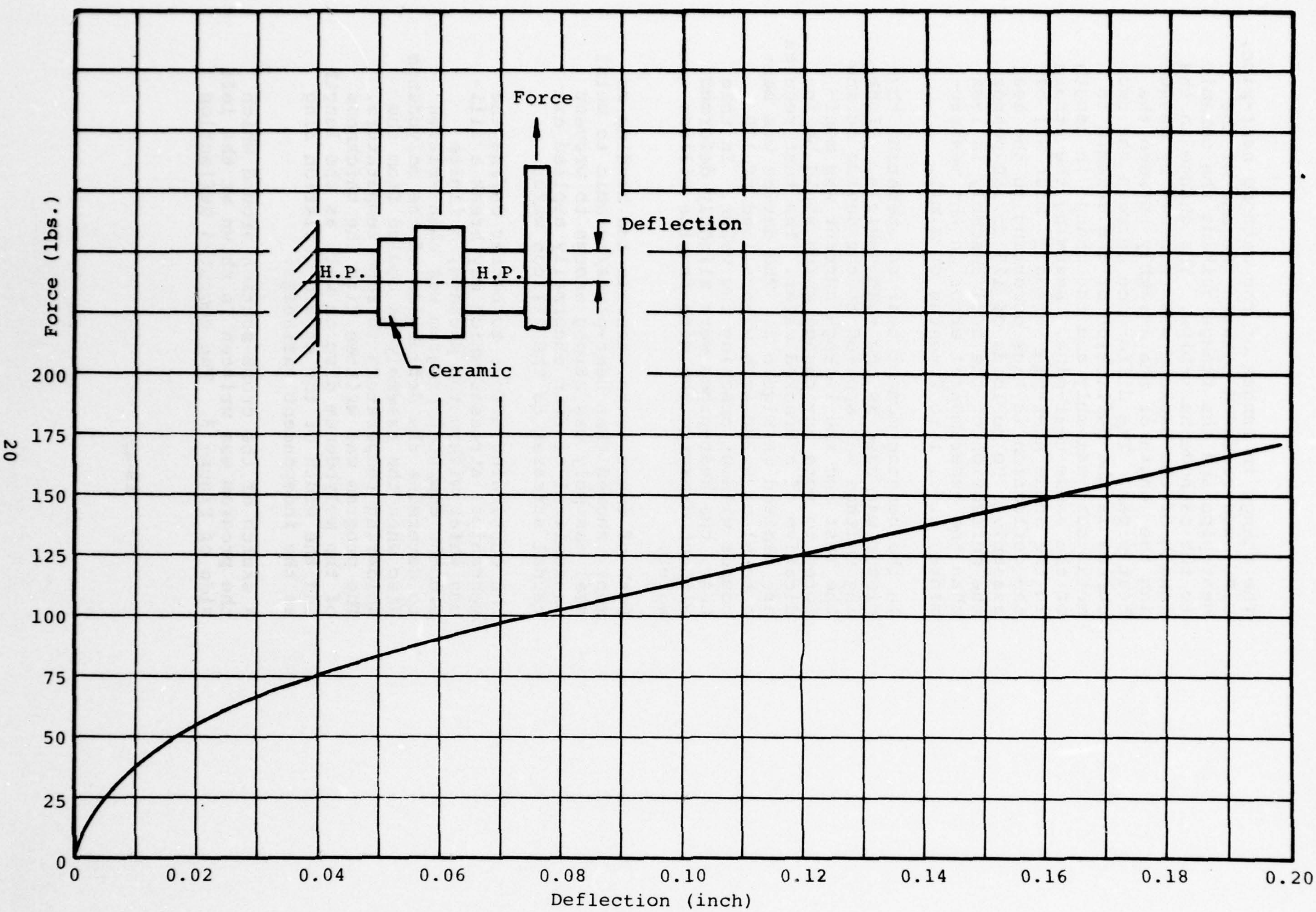


Figure 2 Transcalent Thyristor Bending Moment Test

of the molybdenum from its center to its edge is believed to be a source of the stresses to which the silicon wafer is subjected, after soldering.

The results are graphically presented in Figures 3 and 4. Note that the deflection of the molybdenum decreases rapidly with increasing molybdenum thickness, T_m. Refer to Figure 3. It can be seen that the deflection can be halved by increasing the molybdenum's thickness from 0.030 to 0.040 inch.

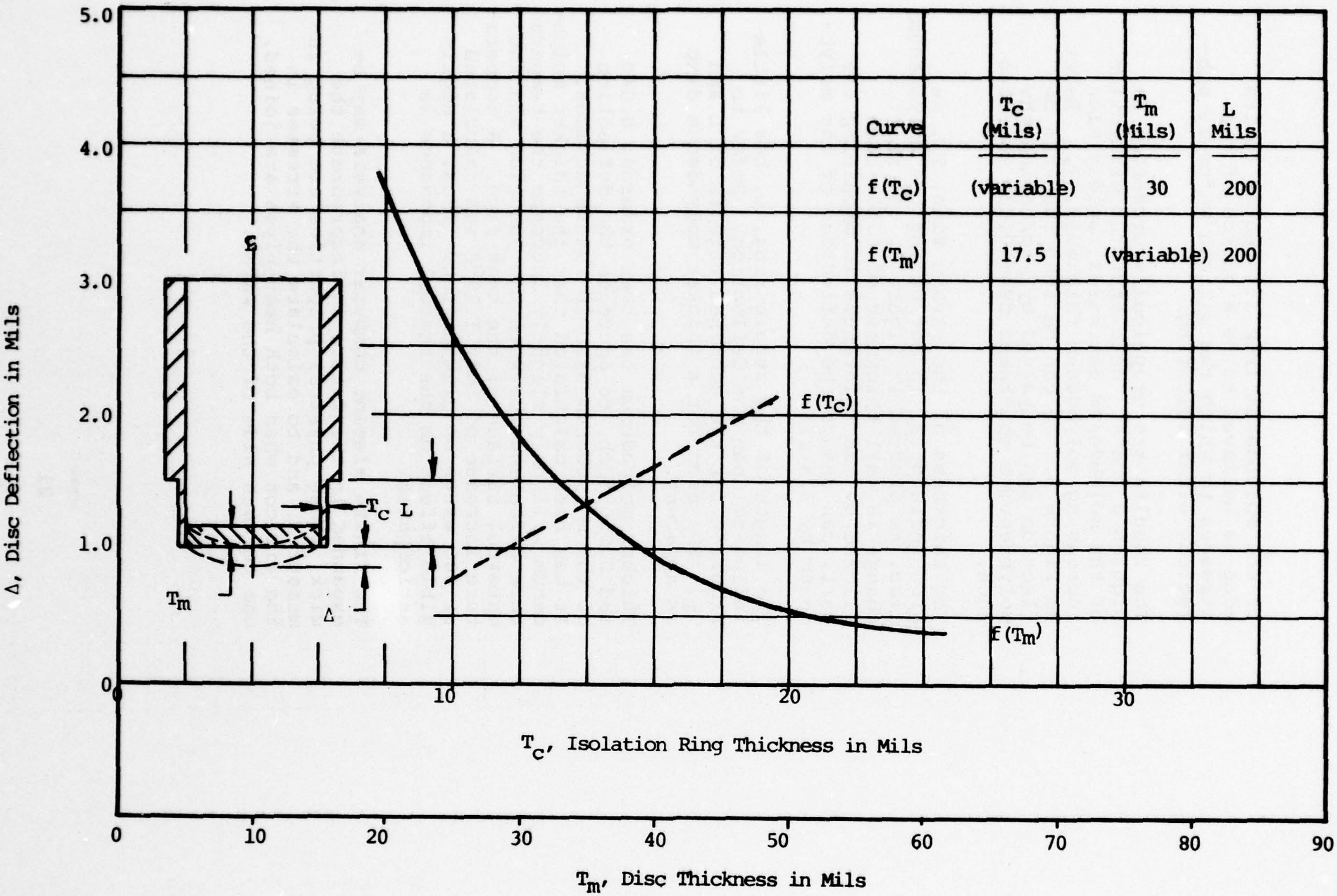
The thickness of the strain ring, T_c, is also influential in deflecting the molybdenum disc, as plotted in Figure 3. In fact, a change in wall thickness of 0.003 inch allowed by the tolerances in machining the part, can change the deflection of the molybdenum by 0.4 mil.

The length of the strain ring, L, has little influence upon the deflection. Refer to Figure 4 for the combined effects of L and T_m. The need for a thicker molybdenum disc is apparent.

Thicker molybdenum has been ordered, 0.040 and 0.050 inch, to decrease the deflection of the molybdenum disc in future devices. It has been calculated that the thicker molybdenum will only slightly increase the temperature difference between the junction and the external surface of the heat-pipe. A temperature increase of only 1.17°C was calculated at 500 watts of dissipation. Thus, a negligible effect on the thermal impedance is anticipated.

The finite element computer analysis may be expanded in the future to incorporate the wick, whose physical properties are being remeasured, and to calculate the stresses in the silicon when both heat-pipes are joined, one to each side of the wafer.

Figure 3 Deflection of Molybdenum Disc as a Function of the Heat-Pipe Dimensions



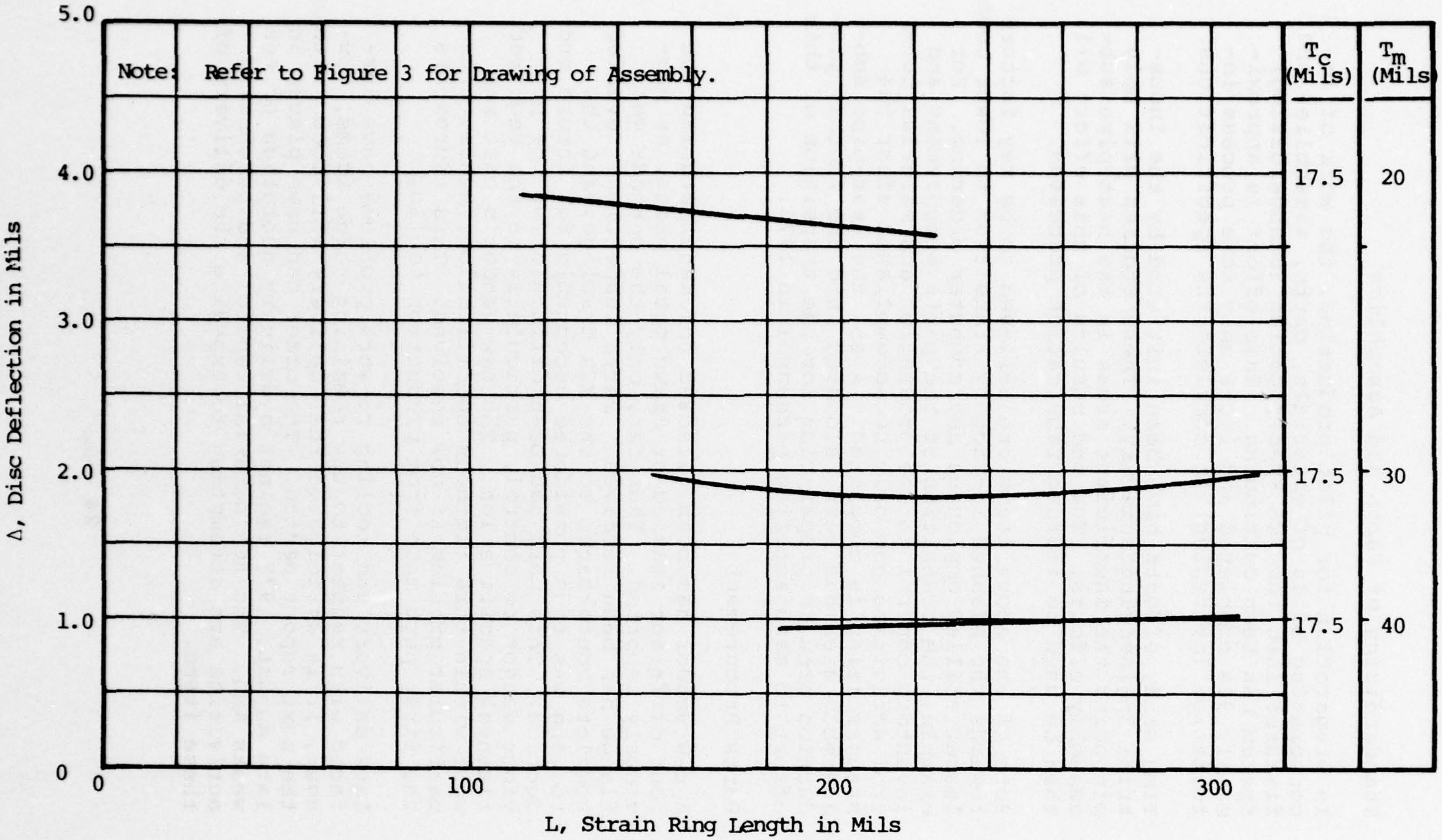


Figure 4 Deflection of the Molybdenum Disc as a Function of the Heat-Pipe Strain Isolation Length

(2) Standardizing of Parts and Assemblies

In preparation for pilot production, the work of incorporating bills of materials, parts, assemblies and fixtures into the RCA specification (standardizing) system has been continuing. This effort is approximately 90% completed and lacks only some process information (at typing) to complete the specifications.

Time study efforts have been initiated by the Industrial Engineering activity. These studies will help pin point the inefficient areas in the heat-pipe subassembly efforts. The end results of this effort will then be used to improve fabrication processes.

Both of the above items are believed to be key factors towards the planned in-factory transition to lower cost, lesser skilled employees and computer ordering. For example, the transition of the parts procurement and inventory control to the production and material control activities can only be accomplished after the standardizing is completed. Also, the heat-pipe subassembly area has been relocated into the factory production area in preparation for the transition of this effort to manufacturing personnel in 1978.

(3) Parts Procurement

A new vendor has been selected for manufacturing the four different stamped or drawn metal parts, as previously reported. Thus far, only the cathode weld flange has been received. Parts inspections revealed complete conformance to the RCA drawings, and the tooling was thus considered acceptable for future production. This part had been difficult for the previous vendor to control, particularly to the required flatness specification. The new vendor's part was well within this flatness specification, hence, this particular problem is now resolved. This represents the first part made from production tooling.

Late delivery and tooling re-work problems have surfaced with respect to the remaining three items, however, it is anticipated that delivery will occur within the next report period. The order had been placed in late August, 1977 against a delivery quotation of ten weeks ARO. The RCA material control and purchasing activities are attempting to expedite the delivery of these items.

(4) Test Plan

Three copies of the test plan, item No. 0005AA, were submitted by DD 250 to Mr. W. R. Peltz on November 21, 1977. The test plan was prepared in accordance with the contract as amended by modification No. P00001.

d. Conclusions

The confirmatory sample phase is proceeding in accordance with the PERT chart. Particular attention is being directed to items that will improve the yield of good thyristor devices. Devices will be tested in accordance with Test Plan for Confirmatory Samples, submitted under a separate cover. Preparations for the pilot production phase are continuing.

e. Drawings

Drawings of the piece parts and sub-assemblies of the device were included in the First Quarterly Report with revisions to these engineering drawings subsequently included in the Second Quarterly Report. Any subsequent revisions will be noted as they occur.

2. Process, Equipment and Tooling

a. Purpose of Each Step

(1) Device Processing and Tooling

Figure 4, Engineering Drawing No. 3025577, in the First Quarterly Report, showed the flow of parts through the various assembly steps and a descriptive title was listed for each operation. Also shown were the sub-assembly drawings and fixture drawing numbers for each operation. In both the First and Second Quarterly Reports, the procedures for using the fixtures were included with a photograph of each fixture. This information continues to be used for the device fabrication and processing.

(2) Electrical and Environmental Test Equipment

The flow chart of the electrical and environmental testing sequence was given in Figure 7, Drawing No. 3025578, of the First Report. The name of the test was given as well as the special conditions and the MIL-STD-750B method number. Long-time tests had the time interval indicated in the figure. This chart remains valid for the program.

b,c. Problem Areas and Work to Resolve Problems

(1) Device Processing and Tooling

Fabrication processes that are known to limit the production quantities are being improved by improving the yields, by increasing the quantity per operation, by reducing the labor required and by more complete documentation of the processes.

(a) Edge Contouring Process Refinement

Rather than waste the high gate current lot #17 wafers, discussed in Part 1.b,c(1) above, they have been sent to an equipment vendor for evaluating his recommended contouring process. The vendor's equipment is capable of cutting both contour angles simultaneously with two sand blast nozzles. This equipment is also able to hold the wafer and the cut-off scarf with a vacuum chuck. Holding the wafer with a vacuum chuck eliminates the time now used for waxing the wafer to a mandrel and then cleaning off the wax after the wafer contouring, thus reducing the contouring cost.

(b) Diffusion Process Refinement

An experimental lot of wafers was processed through boron diffusion to intentionally vary the surface concentration by reducing the times and temperatures at boron deposition. Although the surface resistivity of each group varied at deposition, there was only a slight change in the sheet resistance and in the depth of diffusion following the diffusion drive-in. This experiment was conducted to try to reduce the labor content at the etch back operation. It had been hoped that there would be a shallower gradient in the concentration, thus providing for a reduction in the etching time. Such a gradient was not observed.

The sheet resistances vs. the etching times are plotted in Figure 5 for five different boron deposition schedules. It should be noted that it took 900 to 950 seconds to etch back all of the wafers up to a V/I value in the range of 10 to 15 ohms, regardless of the deposition schedule tried.

(c) Exhaust System Refinements

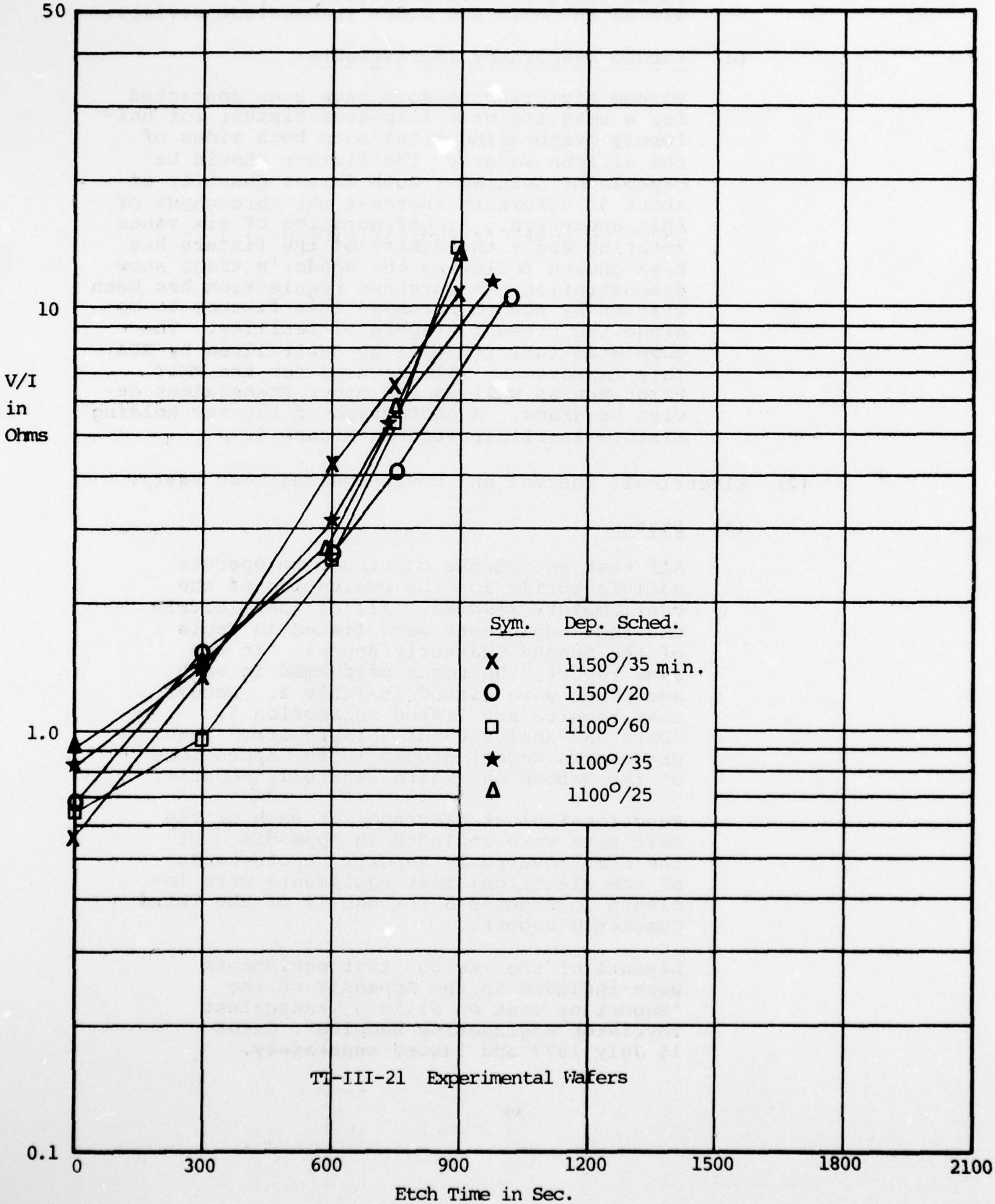
The exhaust and bake-out system for the high voltage center chamber of the device was upgraded from two devices per processing cycle of one-half day to six devices. The new exhaust system was completed in the report period to triple the present exhaust and back-fill process capability to six thyristors simultaneously. To date, it has been used successfully for as many as five devices simultaneously.

(d) Brazing Fixture Procurement

To increase the number of sub-assemblies that can be brazed simultaneously (in keeping with the goals set by the MM&T contract) the quantity of heat-pipe brazing fixtures has been doubled. The outside vendor has delivered all fixturing. Those fixtures that require a non-stick surface are presently being coated and fired for actual use in the brazing furnace.

One problem was noted, however, on the new wicking fixtures which required additional rework. Several key slots in each part required additional grinding and finishing to prevent the possible hang-up of the sintered wick in use. This work has also been completed during the report period.

Figure 5 Wafer Sheet Resistance vs. Etch Back Time



These fixtures were capitalized by RCA for use on the MM&T and other Transcalent Devices.

(e) Vacuum Evaporator Improvements

Vacuum fixturing vendors have been contacted for a rotating or a flip-over fixture for uniformly evaporating metal onto both sides of the silicon wafers. The fixture should be capable of holding a much larger quantity of about 50 wafers to increase the throughput of this operation. A configuration of six vanes rotating about the center of the fixture has been chosen following the vendor's trade show demonstration. A purchase requisition has been written by RCA to purchase this fixture to upgrade the present evaporator facility. The completed facility will be capitalized by RCA. This improvement will be used for the MM&T Pilot Run as well as for other Transcalent device programs. A photograph of the new holding fixture is illustrated in Figure 6.

(2) Electrical, Thermal and Environmental Test Equip.

(a) Status

All test equipments continued to operate satisfactorily for the evaluation of the confirmatory samples. All of the electrical test equipments were listed in Table 1 of the Second Quarterly Report. In the same report, the tests performed in each equipment were listed in Table 2. Actual test results are listed in Section 5, "Data and Analysis" of this report. Test procedures were included in the Appendices of the Second and Third Quarterly Reports.

Functional block diagrams for each of the test sets were included in Appendix C of the First Quarterly Report. Photographs of the electrical test equipments were included in Figures 3 through 12 of the Third Quarterly Report.

Layouts of the various test equipments were included in the Appendix of the "Report of Test on Silicon Transcalent Thyristor Engineering Samples", dated 15 July 1977 and issued separately.

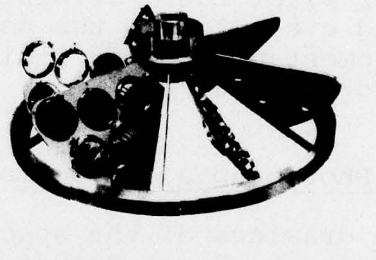


Figure 6 Model 6432 Dual Face Flip Fixture

(b) Test Equipment Calibration Schedules

Electrical test equipment calibration dates were listed in Table 4 of the Fourth Quarterly Report. The schedule established for the recalibration of these equipments on a regular basis was used to recalibrate each equipment in this report period. This call-out occurs automatically at four to six months intervals. The calibration was carried out by the RCA Meter Laboratory Calibration and Standards Dept.

Environmental test equipment calibrations in the RCA-Lancaster environmental laboratory are also performed at four to six months intervals. The calibration schedule was listed in Table 5 of the Fourth Quarterly Report.

d. Conclusions

The process, equipment and tooling designed, fabricated and used to fabricate and evaluate the engineering sample devices is now being used for the initial confirmatory sample devices. The throughput of some of the equipment has been or is being increased for the confirmatory sample phase and for the larger pilot run. Several addtional devices will be fabricated and evaluated in the next report period. No process, equipment or tooling limitations are apparent for the confirmatory phase.

e. Drawings and Photographs of Tooling and Equipment

Copies of the drawings of the special tools and fixtures were included in the First Quarterly Report along with Block Diagrams of the test equipment. Tools and fixtures that were revised were included in the Second Quarterly Report. Photographs of these items were included in both reports.

Photographs of the electrical test equipment were included in the Third Quarterly Report with text references that described each equipment item. Testing procedures for the electrical test equipment were included in Appendix C of the Second Quarterly Report and in the Appendix of the Third Quarterly Report.

3. Flow Chart of Manufacturing Process Yield

Manufacturing process yields are to be determined during the Pilot Run.

4. Equipment and Tooling Costs

This information will not be included since such a data requirement is generally not applicable to a Firm Fixed Price Contract on equipment and tooling that is purchased and furnished by the contractor for unrestricted use in fabricating the devices required by the contract.

5. Data and Analysis

a. Inspections

(1) Confirmatory Sample Devices

These devices are being inspected in accordance with paragraph 4.4, using the sampling plan included in this paragraph of SCS-477. The requirements of paragraphs F.48 of the contract and 1.2.6 and 3.1.8 of ECIPPR No. 15 are also being observed.

Initial test results on the first five confirmatory samples are listed in TABLES la, b, c and d. Additional devices will be tested in the next report period, as soon as fabrication is completed. Only device N18 remains fully operable from the initial group of samples.

The data for the spare engineering sample device No. N10 is repeated in the table for comparison with the newer devices. Also, additional tests performed on N10 in this report period have been added for reference.

TABLE 1a TEST DATA RECORD FORMS - CONFIRMATORY SAMPLE DEVICES

ITEM: SILICON TRANSCALENT THYRISTOR, J15371 | CONTRACT: DAA B07-76-C-8120 |

SPEC: SCS-477   5 DECEMBER 1974 &   AMENDMENT - 1   31 AUGUST 1976

MFR: RCA (EO&D) LANCASTER, PA.

BUYER: COMM.SYS.PROCUREMENT BRANCH (USAECOM), FT.MONMOUTH, N.J.

GROUP	A											
SUBGROUP	1	2	2	4	4	4	3	3	3	3	4	4
NO.UNITS TESTED	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
TEST	Visual & Mech.	Reverse Current	Forward Blocking	Gate Trig.V	Gate Trig.I	Holding Current	Reverse Current	Forward Block'g	Gate Trig.V	Exp.Rate V Rise	Turn-off Time	On State Voltage
MIL-STD-750 METHOD	2071	4211	4206	4221	4221	4201	4211	4206	4221	4231	4224	4226
TEST CONDITION	Visual Inspt.	25°C →					125°C →				25°C →	
SYMBOL	-	i_{RBOM}	i_{FBOM}	V_{GT}	I_{GT}	I_H	i_{RBOM}	i_{FBOM}	V_{GT}	dv/dt	t off	V_{FM}
MAX.	-	15mA	15mA	5Vdc	1.0 Adc	500mAdc	60mA	60mA	5.0Vdc		150µs	2.0V
MIN.	-									100 V/µs		
3rd & 4th Q 1977 Date Tested / UNIT NO.	ACC REJ											
N12	✓	0.2	0.2	0.8	80	1	2	6	0.4	253*		1.1
N13	✓	0.2	0.1	1.1	400	1	3	5	0.6	361*	57	1.2
N16	✓	0.4	0.5	1.1	780	8	13	38	0.6	281Δ	46	1.1
N17	✓	0.3	0.6	1.2	720		24	47	0.7	281Δ		1.1
N18	✓	0.5	1.6				30	50				
N10 (Prior Data)	✓	0.3	0.5	1.1	160	8	28	41	0.5	422*	36	1.3

*Tested @ $T_C = 125 {}^{+0}_{-3}$ °C, V_{AA} = 800 v and Gate Condition B.

ΔTested @ $T_C = 125 {}^{+0}_{-3}$ °C, V_{AA} = 800 v and Gate Condition D.

Note: Details of test conditions are given in spec. SCS-477.

TABLE 1 b

CONTR'S. TYPE: J15371 DATE TEST COMPLETED: SAMPLE NOS. Page 2 of 4

MFR'S. TYPE: J15371 DATE TEST BEGUN: FR. 8/77 TO

B													
1	1. Final Measurements			2			3. Final Meas.		4. Final Measurements				
10%	10%	10%	10%	100%	100%	100%	10%	10%	10%	10%	10%	10%	
Surge Current	Reverse Current	Forward Block'g	Rev. Gate Current	Gate Trig. V	Gate Trig. I	On-state Volt.	Temp. Moist	Cycle & Resist	Blocking per para.	Voltage 4.6.1	Life	Test	
4066	4211	4206	4219	4221	4221	4226	1051	1021	4211	4206	4211	4206	
→ 25°C	25°C →		→	-25°C →		→	4211	4206 →	25°C →		125°C →		{case {temp, T_C
I_{FM}	i_{RBOM} 15mA	i_{FBOM} 15mA	I_{GR} 7.0 A pulsed	V_{GT} 10Vdc	I_{GT} 1.5Adc	V_{FM} 2.3V	i_{RBOM} 15mA	i_{FBOM} 15mA	i_{RBOM} 15mA	i_{FBOM} 15mA	i_{RBOM} 60mA	i_{FBOM} 60mA	
10 Surges													
4,000 A pk													
N12 10+	0.2	0.2	0.5	(Frozen but not tested)									
N13 12	0.2	0.2	0.4	1.1	100	1.2							
N16 10	0.4	0.5	3.8	1.2	990	1.1			20#	0.5			
N17													
N18													
N10	0.3	0.6	0.8	1.2	250	1.3	<0.1	<0.1	0.7##	1.5##	35##	50##	

#At a degraded reverse voltage of 366 v. following 140 hours of the Blocking Voltage Life Test.

##Blocking Voltage Life Test repeated for over 592 more hours at 81% to 88% peak voltage and $T_C = 122^oC$. Total accumulated time = 767 hours.

TABLE 1c

GROUP	C									
SUBGROUP	1					2.Final Measurements				
NO.UNITS TESTED	100%	100%	100%	100%	100%	10%	10%	10%	10%	10%
TEST	Physical Dimens.					Shock,	Vibration,	Constant	Accel.	
MIL-STD-750 METHOD	2066					2016	2056	2006		
TEST CONDITION	Figure 1					4211	4206	4221	4221	4226
SYMBOL	A	B	C	D	E	i_{RBOM}	i_{FBOM}	V_{GT}	I_{GT}	V_{FM}
MAX.	5.00"	3.475"	0.700"	1.857"		20mA	20mA	5Vdc	500mAdc	2.5V
MIN.		3.425"	0.600"		6.00"					
								For information only - Not a spec. requirement		
UNIT NO.										
N12										
N13										
N16										
N17										
N18										
N10	4.88@	3.440@	0.656@	1.806@		0.2	0.4	0.9	160	1.4

@Added data recorded since Oct. 1, 1977. Other N10 results are repeated from Table 6 of the Fourth Quarterly Report.

TABLE 1d

	3. Final Measurements					4. Final Measurements					5		$A^{\Delta\Delta}$ $3^{\Delta\Delta}$
	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	100%		100%
	Reduced Barometric Pressure					Salt Atmosphere, Thermal Fatig.					Thermal Resistance		Gate Trig. I
	1001					1041	para. 4.6.2				3151		4221
	4211	4206	4221	4221	4226	4211	4206	4221	4221	4226			125^oC
	i_{RBOM}	i_{FBOM}	V_{GT}	I_{GT}	V_{FM}	i_{RBOM}	i_{FBOM}	V_{GT}	I_{GT}	V_{FM}	θ_{J-c}		I_{GT}
	20mA	20mA	5Vdc	500mAdc	2.5V	20mA	20mA	5Vdc	1.0 Adc	2.5V	0.15^oC/Watt		
	15 mm Hg 800 V.pk										250 Adc		
											Initial$^{\Delta\Delta}$	Final	
N12	0.2	0.2	0.8	80	1.3						0.13		20 mA
N13	0.2	0.2	0.8	70	1.2						0.14		100
N16											0.14		400
N17											0.11		320
N18													
N10	0.2	0.5	0.9	160	1.4	0.2	0.4**	0.9**	160**	1.4**	0.08	0.09	50[@]

$^{\Delta\Delta}$Tests added per paragraph 3 of modification No. P00002 to the contract.

**Following Thermal Fatigue Test, only.

[@]Added data recorded since Oct. 1, 1977. Other N10 results are repeated from Table 6 of the Fourth Quarterly Report.

b. Discussion of Inspection Results

The initial test results on the five devices built thus far in the Confirmatory Sample phase reveal an obvious consistency and reproducibility of most of the electrical and thermal characteristics. The basic device design is thus judged to be adequate. Specific comments, analysis and discussion of the test results are listed below by inspection sub-group in SCS-477. Refer to TABLE 1a, b, c and d for both the specifications (spec.) and the actual measured values.

(1) TABLE I - Group A Inspections

All units are to be tested to all four sub-groups of TABLE I.

(a) Sub-Group 1

All devices were acceptable at Visual and Mechanical inspection.

(b) Sub-Group 2

The room temperature forward and reverse blocking currents at 800 volts were all well within the spec.

(c) Sub-Group 3

Improvement in the forward and reverse leakage current characteristics has occurred at 125°C, comparable to N10. The gate voltages are well within spec. and the dv/dts at the high temperature of 125°C are satisfactory.

(d) Sub-Group 4

The gate trigger voltages, holding currents and on-state voltages are all in spec. The gate currents and turn-off times were well within the spec. on all of the devices also.

(2) TABLE II - Group B Inspections

(a) Sub-Group 1

This surge test of one unit will be performed also on a randomly selected sample in the next report period.

(b) Sub-Group 2

All units must pass these gate trigger and on-state tests at 25°C below zero. Both N12 and N13 failed following these tests. They will be replaced with improved units.

(c) Sub-Group 3

These environmental tests of temperature cycling and moisture resistance will be performed on a randomly selected sample in the next report period.

(d) Sub-Group 4

Device No. N16 degraded after 140 hours of this blocking voltage life test. It has been learned subsequently that unregulated high voltage without adequate grounding was used for the test. This erratic test condition undoubtedly subjected the unit to excessive voltages and thus may have contributed to the premature failure of the unit. N16 also operated unattended for several hours in a breakdown mode without the protective fuse blowing. This condition undoubtedly exceeded a safe operating temperature for the junction because of the increased dissipation in the device.

The subsequent retest of N10 for 592 hours was completed satisfactorily. Final measurements are listed.

Another unit will be randomly selected in the next report period for the performance of this test under the proper controlled conditions.

(3) TABLE III - Group C Inspections

(a) Sub-Group 1

All devices to be submitted as confirmatory samples will be inspected for physical dimensions in the next report period. Recent measurements on N10 are listed for reference.

(b) Sub-Group 2

A random sample unit will be subjected to the shock, vibration and constant acceleration tests in the next report period. Since the latter test is for information only, it may be performed with a non-shippable unit.

(c) Sub-Group 3

This reduced barometric pressure test will also be performed on a randomly selected unit in the next report period.

(d) Sub-Group 4

These salt atmosphere and thermal fatigue tests will be performed on a randomly selected unit in the next report period.

(e) Sub-Group 5

This thermal resistance test has been performed on each unit before the -25°C tests of Table II, Sub-Group 2. All passed, but unit N17 was found to have failed following this test. N17 will be replaced with a new unit.

This test will also be performed on all units after the -25°C tests.

c. Special Tests

Some additional special tests were performed also on these initial confirmatory sample devices to assist in the interpretation of the results and to guide realistic ratings.

(1) Instantaneous Forward Characteristics

These peak voltage and current characteristics were measured on device No. N12 up to 4,100 amperes. This data is useful for projecting both the surge and the overload capabilities. Note the more normal operation at the 400 amperes RMS maximum rating is well down on the curve of Figure 7.

(2) Isothermal Characteristics

Verification that both heat-pipes are functioning properly can be secured by measuring the temperature uniformity along the finned length of each pipe and by comparing the two pipes. This data is plotted in Figure 8 for device No. N13 for two current values. The temperature was measured at the base of the fins on the outer wall of the heat-pipe. Note good uniformity exists within a few percent.

Figure 2 Instantaneous Forward Voltage and Current Characteristics - J15371 #N12

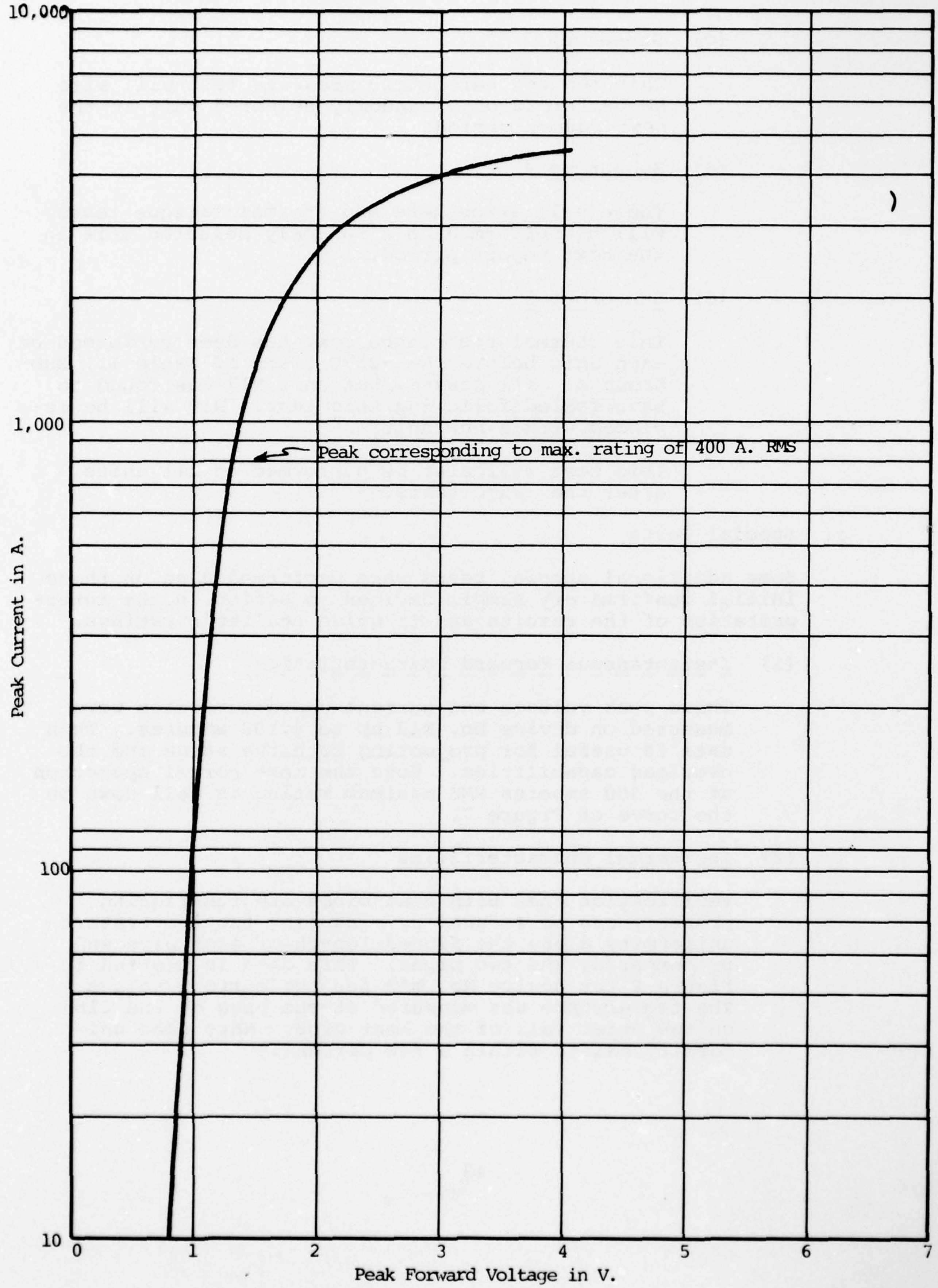
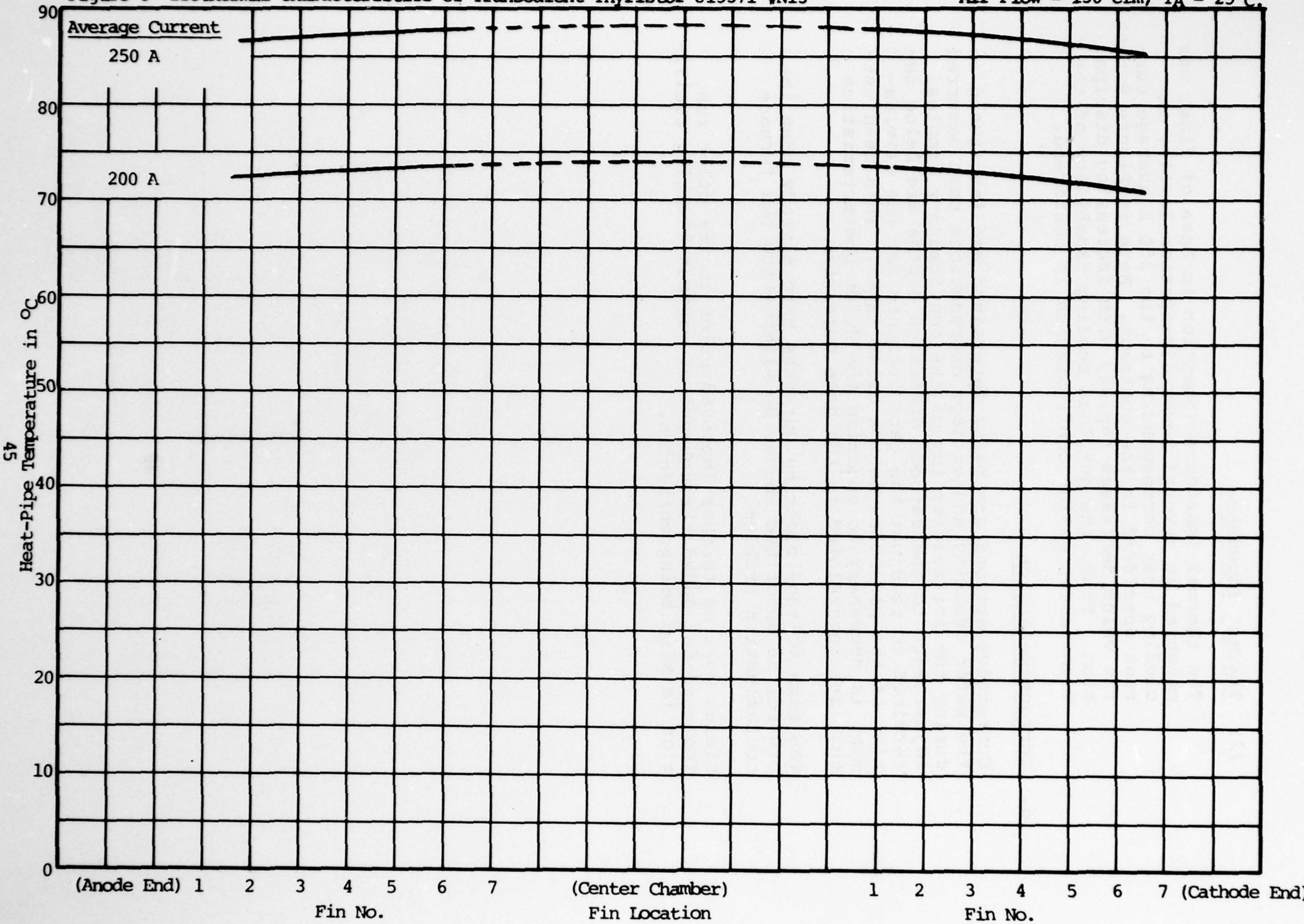


Figure 8 Isothermal Characteristics of Transcalent Thyristor J15371 #N13



(3) Thermal Impedance

The thermal impedance (junction to base of fins) was measured at several power dissipation levels, including that corresponding to the 250 A average current specified in the contract. Note in Figure 9 that the value decreases rapidly with increasing dissipation. Thus, the overload cooling capability of the Transcalent design configuration is confirmed.

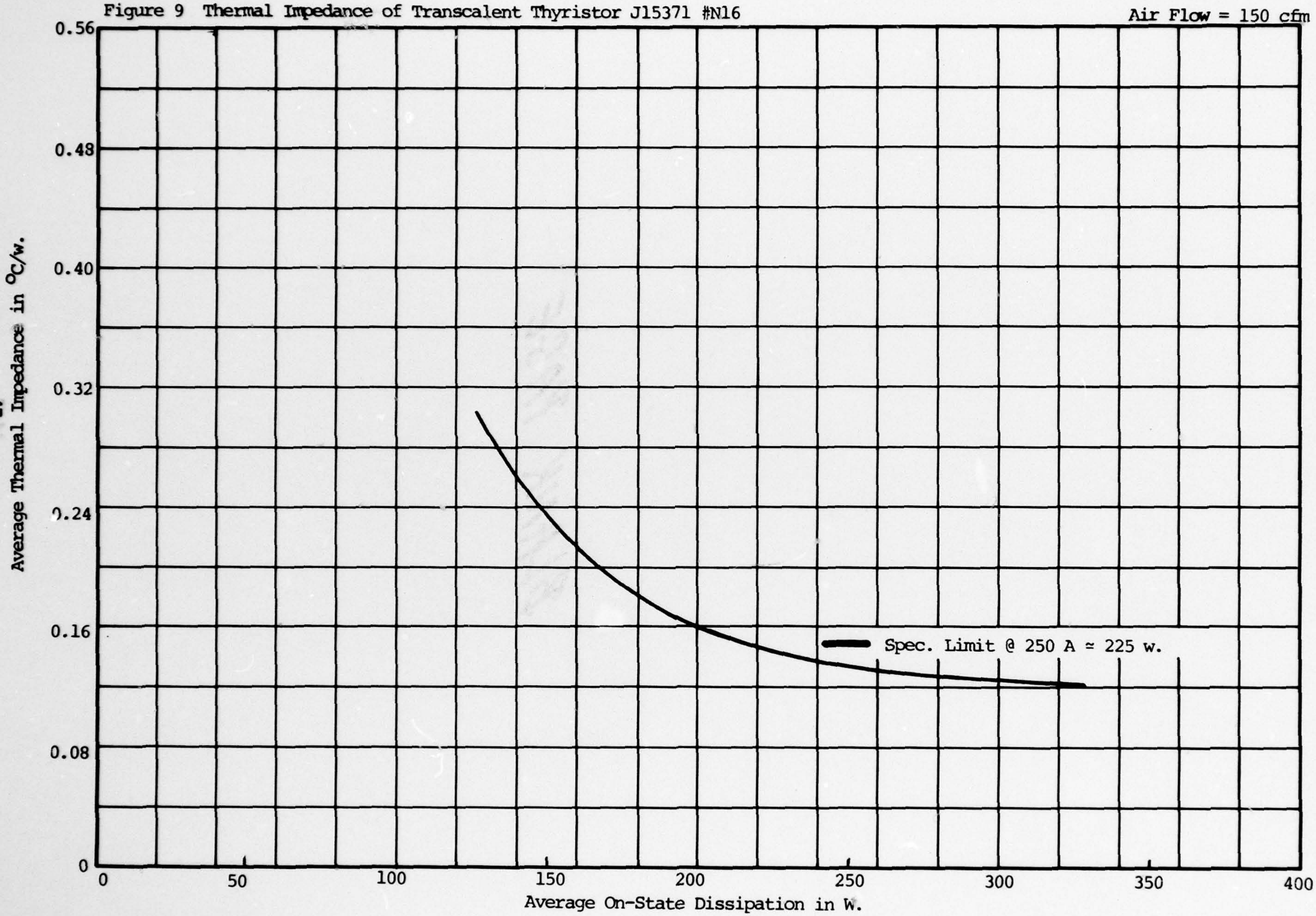
d. Corrective Action

Corrective actions are being determined and instituted on the wafer cracking and voltage degradations that occurred during the initial testing of the confirmatory samples. Adjustments to the cathode diffusion depths are being determined to readjust the gate currents for the elimination of the pin-holes in the oxide layer. This readjustment is necessary to optimize the dv/dt characteristics that are interelated to the gate currents.

The high voltage blocking currents have already been improved, as described above, by eliminating the furnace contamination problem.

Yields must be further improved prior to the pilot run. The need for added through-put of various limiting facilities is also being corrected.

Figure 9 Thermal Impedance of Transcalent Thyristor J15371 #N16



6. Specification

The 13 October, 1977 specification changes suggested as consideration for the schedule change included the addition of a preliminary thermal resistance test of TABLE III, Sub-Group 5 and a gate trigger current test of TABLE I, Sub-Group 3. The first provides a preliminary determination of heat-pipe efficiency which could then be used to detect any internal damage, or delamination that may be caused by the frozen start (-25°C) test of TABLE II, Sub-Group 2. The second adds a high temperature measurement of the gate trigger current. These added tests will be performed on all of the confirmatory sample and pilot run devices. These changes will be issued as modification No. P00002 in the next report period.

Another specification change is related to the dv/dt limits and test conditions, as described in a 30 September, 1977 proposal for modification. This modification is being used for the confirmatory sample devices since these test specification changes were incorporated in the Test Plan for the confirmatory samples, as submitted 21 November, 1977. Approval of both submissions is awaited.

Any further modification of the specifications of SCS-477 is not recommended at this time.

7. Requirement for Pilot Run

Not applicable until later in the contract.

8. Total Cost for Pilot Run

Data not available until the pilot run is completed.

9. Program Review

The PERT Chart revision submitted 29 August 1977 remains in effect showing a mid-March, 1978 completion date for the confirmatory phase.

CONCLUSIONS

Effort expended in the fifth contract quarter was successful in initiating the Confirmatory Sample phase with five devices fabricated, to date. Verification that the SCR engineering design meets all but one specification requirement adds assurance that the Confirmatory Sample phase should also be successful. Corrective action as well as a proposed specification modification should alleviate the one limitation on subsequent devices. RCA is thus confident of meeting the full MM&TE specification requirements for the confirmatory sample and pilot run devices. Both improved wafers and improved packages are being fabricated for these devices.

Fabrication of the Confirmatory Samples has begun under the authorization dated 15 August, 1977. Preparations for production will be evaluated during this phase to reveal any limitations that need to be corrected prior to the pilot run. The program is proceeding in accordance with the revised PERT Chart, 29 August, 1977.

PROGRAM FOR THE NEXT QUARTER

1. Complete the fabrication and evaluation of the Confirmatory Sample devices using low leakage current wafers,

2. Proceed under the assumption that both the Test Plan and the dv/dt specification modification will be approved in writing,

3. Issue the monthly reports, as required by DD 1423,

4. Submit the five confirmatory samples and the corresponding test report, and

5. Continue to improve facility through-put limitations in preparation for the Pilot Run phase.

IDENTIFICATION OF PERSONNEL

The professional and skilled technical personnel who actually worked on the MM&TE project during the first five quarters of the contract had varied backgrounds, as listed in the biographical resumes included in the previous Quarterly Reports. No additional resumes are included in this report since no additional members of the technical staff were assigned to the project in the Fifth Quarter.

However, a management decision was implemented to establish a silicon technology center in the Electro-Optics activity of the Lancaster plant. Refer to Figure 10 for the revised organization chart. All wafer diffusions for the MM&T devices are now the responsibility of this new activity. The availability of a high volume, semi-automated production facility in the technology center was a consideration in the reassignment of the diffusion engineering responsibilities from Power Products to E.O. The E.O. personnel were involved previously in the MM&T program on a part-time basis.

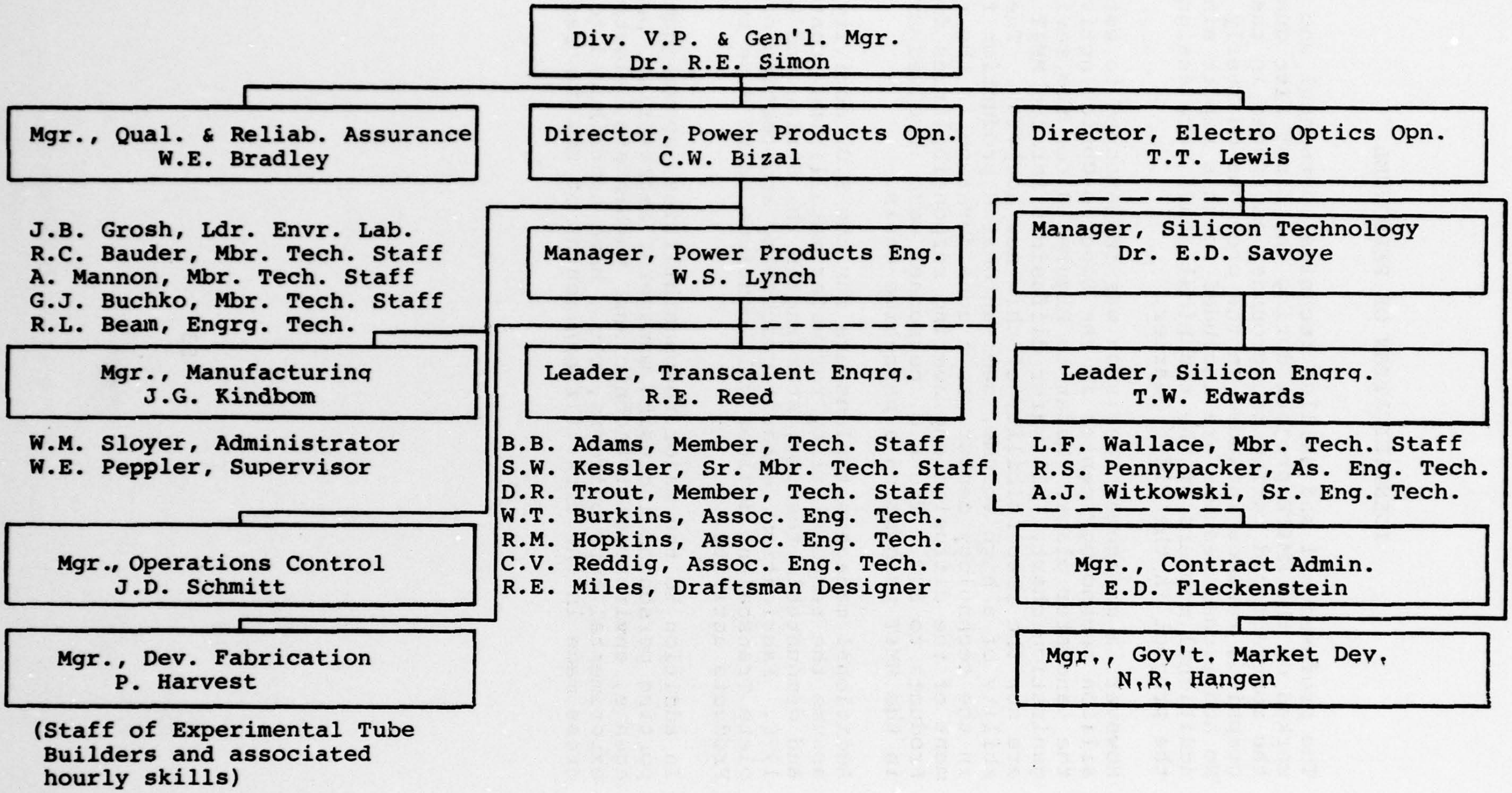
Additional management plans are for the E.O. activity to also assume the responsibility for wafer metallizing, contouring and demountable testing, starting in the Spring and Summer of 1978. Fabrication, exhaust processing and testing of the complete Transcalent devices will continue to be done by the Power Products activity.

In addition to the major responsibilities, above, numerous supporting personnel including managers, secretaries, purchasing agents, environmental technicians, machinists, electricians, experimental tube builders, etc., have contributed to the progress made in the first fifteen months of the contract.

TECHNICAL ORGANIZATION CHART
Electro Optics and Devices

Contract DAAB07-76-C-8120

Figure 10 MM&T PROGRAM FOR TRANSCALENT THYRISTOR



Note: Dashed lines indicate functional reporting responsibilities.

DISTRIBUTION LIST

The following pages include the distribution list supplied by the contracting officer with the approval letter for the First Quarterly Report as well as the additions authorized subsequently.

This list was utilized also for the distribution of the Second, Third and Fourth Quarterly Reports.

DISTRIBUTION OUTSIDE OF RCA-SSD

Dr. Paul E. Greene
Dir. Solid State Lab.
Hewlett Packard Co.
1501 Page Mill Road
Palo Alto, CA 94304

Mr. Gerald B. Herzog
Staff Vice President
Technology Centers
RCA
David Sarnoff Res. Ctr.
Princeton, NJ 08540

Dr. George E. Smith
Bell Telephone Labs, Inc.
MOS Device Dept.
600 Mountain Ave.
Room 2A323
Murray Hill, NJ 07974

Commander
U.S. Army Electronics Command
ATTN: DRSEL-TL-1
Mr. Robert A. Gerhold
Fort Monmouth, NJ 07703

Commander
Harry Diamond Labs.
2800 Powder Mill Rd.
ATTN: DRXDO-RCC,
Mr. Anthony J. Baba
Adelphi, MD 20783

Commanding Officer
Picatinny Arsenal
ATTN: SARPA-ND-D-A-4
Mr. Arthur H. Hendrickson
Bldg. 95
Dover, NJ 07801

Commanding General
U.S. Army Missile Command
ATTN: Mr. Victor Ruwe,
DRSMI-RGP
Redstone Arsenal, AL 35809

Commander
U.S. Army Electronics Command
ATTN: DRSEL-TL-BS
Mr. George W. Taylor
Fort Monmouth, NJ 07703

Commanding Officer
U.S. Army Research Office
P.O. Box 12211
ATTN: Dr. Chas. Boghosian
Research Triangle Park, NC 27709

Naval Research Laboratory
ATTN: Dr. David F. Barbe,
Code 5260
4555 Overlook Avenue, SW
Washington, DC 20375

Naval Electronics Lab Center
ATTN: Mr. Charles E. Holland, Jr.
Code 4300
271 Catalina Blvd.
San Diego, CA 92152

The Johns Hopkins Univ.
Applied Physics Laboratory
ATTN: Dr. Charles Feldman
11100 Johns Hopkins Road
Laurel, MD 20810

Commander
Naval Surface Weapons Center
ATTN: Mr. Albert D. Krall,
Code WR-43
White Oak
Silver Spring, MD 20910

Commander
RADC
ATTN: Mr. Joseph B. Brauer, RBRM
Griffiss AFB, NY 13441

NASA
Geo. C. Marshall Space Flight Center
ATTN: Dr. Alvis M. Holladay, Code EC-41
Marshall Space Flight Center, AL 35812

NASA
Langley Research Center
Langley Station
ATTN: Mr. Charles Husson, M/S 470
Hampton, VA 23665

Dir. National Security Agency
ATTN: Mr. John C. Davis, R55
Fort George C. Meade, MD 20755

Commander
U.S. Army Production
Equipment Agency
ATTN: AMXPE-MT
(Mr. C. E. McBurney)
Rock Island, IL 61201

Mr. Jack S. Kilby
5924 Royal Lane
Suite 150
Dallas, TX 75230

Dr. Barry Dunbridge
TRW Systems Group
One Space Park
Redondo Beach, CA 90278

Mr. Harold D. Toombs
Texas Instruments, Inc.
P.O. Box 5474; M/S 72
Dallas, TX 75222

Commander, AFAL
ATTN: AFAL/DEH
Mr. Stanley E. Wagner
Wright Patterson AFB,
OH 45433

Lincoln Laboratory, MIT
ATTN: Dr. Donald J. Eckl
P.O. Box 73
Lexington, MA 02173

RADC (ETSD)
ATTN: Mr. Sven Roosild
Hanscom AFB, MA 01731

General Electric Company
Semi-Conductor Products Dept.
Building 7, Box 42
Syracuse, NY 13201

Micro-Electronics Laboratory
Hughes Aircraft Company
500 Superior Avenue
Newport Beach, CA 92663

Silicon Transistor Corp.
ATTN: Mr. P. Fitzgerald
Katrina Road
Chelmsford, MA 01824

Mr. Daniel Becker
Reliability & Qual. Test Center
Mannes Spacecraft Center
Houston, TX 77058

Texas Instruments, Inc.
Library M.S. 20
P.O. Box 5012
Dallas, TX 75222

Dr. S. Bakalar
Transitron Electronic Corp.
168 Albion Street
Wakefield, MA 01880

Mr. R. Riel
Westinghouse Electric Corp.
R&D Center
Pittsburgh, PA 15235

National Semi-Conductor Corp.
Attn: Mr. R. Bregar
Danbury, CT 06810

Solitron Devices
256 Oak Tree Road
Tappan, NY 10983

Dr. L. Suelzle
Delta Electronics Corp.
2801 S. E. Main Street
Irvine, CA 92714

Bell Laboratories
ATTN: Mr. W. H. Hamilton
Whippany Road
Whippany, NJ 07981

Commander
Naval Ships Res. & Dev. Center
ATTN: W. Kohl (Bldg. 100-3)
Annapolis, MD 21402

Power Systems Division
ATTN: Mr. Kenneth Lipman
Box 109
South Windsor, CT 06074

Martin Marietta
ATTN: Mr. E. E. Buchanan
P.O. Box 179
Denver, CO 80201

J. J. Henry Co., Inc. Special Proj.
Attn: Mr. Mike Saboe - NSRDC Study
2341 Jefferson Davis Highway
Arlington, VA 22202

Fermi National Accelerator Lab.
ATTN: Mr. Frank S. Cilyo
P.O. Box 500
Batavia, IL 60510

Hughes Aircraft Company
Ground Systems Group
ATTN: Dr. Kal Sekhon
Fullerton, CA 92634

Commander
Navy Weapons Center
ATTN: Mr. S. S. Lafon
China Lake, CA 93555

Commander (2)
U.S. Army Electronics Command
ATTN: DRSEL-PP-I-PI
Mr. William R. Peltz
Fort Monmouth, NJ 07703

Commander (2)
U. S. Army Mobility Equipment
Research and Development Ctr.
ATTN: STSFB-EA
Dr. Russ Eaton
Fort Belvoir, VA 22060

Advisory Group on Electron Dev. (2)
ATTN: Working Group on Pwr. Devices
201 Varick Street
New York, NY 10014

Mr. Ron Wade
ATTN: ELEX-0151431
Naval Electronic Sys. Command
Washington, DC 20360

Dr. Robert Redicker
Mass. Inst. of Technology (MIT)
Building 13-3050
Cambridge, MA 02139

Defense Electronics Supply Ctr.
Directorate of Engineering
and Standardization
DESC-ECS (Mr. N. Hauck)
1507 Wilmington Pike
Dayton, OH 45401

General Instrument Corp.
Semi-Conductor Prod. Group
ATTN: Mr. G. Cohen
600 W. John Street
Hicksville, LI, NY 11802

Harry Diamond Laboratories
ATTN: Technical Library
Connecticut Avenue and
Van Ness Street
Washington, DC 20438

Jet Propulsion Laboratory
ATTN: Mr. L. Wright
Mail Stop 158-205
4800 Oak Grove Drive
Pasadena, CA 71103

NASA
Lewis Research Center
ATTN: Mr. Gail Sundberg (MS54-4)
2100 Brook Park Road
Cleveland, OH 44135

Commander
AF Aero Propulsion Lab.
ATTN: AFAL/PODI
(Mr. Philip Herron)
Wright Patterson AFB OH 45433

Commander
Naval Air Development Center
ATTN: Mr. Howard Ireland (3043)
Mr. Joseph Segrest
Warminster, PA 18974

Commander
NAVSEC Code 420 CTRBG
ATTN: Mr. Arnold D. Hitt, Jr.
801 Center Building
Hyattsville, MD 20782

Delco Electronics
ATTN: Dr. A. Barrett
Mail Code 8106
676 Hollister Avenue
Goleta, CA 93017

NASA
Johnson Space Center
ATTN: Mr. E. Wood, Code EG2
Houston, TX 77058

Garrett Air Research Mfg. Co.
of Arizona
ATTN: Mr. R. N. McGinley
P.O. Box 5217
402 S. 36th Street
Phoenix, AZ 85010

Lockheed California Co.
ATTN: Mr. W. W. Cloud
Department 75-82
Bldg. 63/3, Box 551
Plant A-1
Burbank, CA 91520

Sanders Associates
ATTN: Mr. A. Hurley
NCAI - 6247
95 Canal Street
Nashua, NH 03061

Defense Documentation Center (12)
ATTN: DDC-IRS
5010 Duke Street
Cameron Station (Bldg. 5)
Alexandria, VA 22314

NASA
Scientific & Tech. Inf. Off./KSI
Washington, DC 20541

Commander
U.S. Army Electronics Command
Communications Systems
Procurement Branch
Fort Monmouth, NJ 07703
ATTN: Capt. H. John Patch/PCO
DRSEL-PP-C-CS-1

TRW, Inc.
Defense & Space Systems Group
ATTN: Mr. Art Schoenfeld
One Space Park
Redondo Beach, CA 90278

Garrett Air Research
ATTN: Mr. Everett Geis
2525 West 190 Street
Torrance, CA 90509

Airesearch Manufacturing Co.
ATTN: Mr. John Ashmore
Electronic Systems
2525 W. 190th Street
Torrance, CA 90509

Naval Underwater Systems Center
ATTN: Mr. George Anderson/Code 3642
Newport, RI 02840

Dr. Roy Scott Hickman
Chairman, Dept. of Mech.
and Environ. Engrg.
University of California
Santa Barbara, CA 93106

DISTRIBUTION WITHIN RCA-SSD

Dr. R. E. Simon
055-191

C. W. Bizal
057-631

W. S. Lynch
057-631

E. D. Fleckenstein
053-460

N. R. Hangen (2)
073-637

S. W. Kessler
086-963

D. R. Trout
086-963

W. T. Burkins
086-963

C. V. Reddig
086-963

A. J. Witkowski
086-963

R. M. Hopkins
086-963

R. E. Reed (10)
086-963

R. Glicksman - Somerville

E. D. Savoye
073-632

T. Edwards/F. Wallace
089-980

J. Grosh/R. Bauder
080-923

G. J. Buchko/R. Beam
003-953

R. F. Keller
086-963

H. F. Lebegern
068-682

Library
686

R. M. Bowes
057-631

J. G. Kindbom/W. Peppler
003-953

W. M. Sloyer
003-953

J. V. Platt
Somerville

C. Turner
Somerville

K. C. Harding
Arlington

E. Schmitt
Somerville

B. B. Adams
086-963